Single Channel, 1024-Position, 1% R-Tol, Digital Potentiometer

Preliminary Technical Data

AD5293

FEATURES

Single-channel, 1024-position resolution
20 kΩ, 50 kΩ and 100 kΩ nominal resistance
Calibrated 1% Nominal Resistor Tolerance
Rheostat mode temperature coefficient: 35 ppm/°C
Voltage divider temperature coefficient: 5 ppm/°C
+21V to +30V single-supply operation
±10.5V to ±15V dual-supply operation
SPI® compatible serial interface
Wiper setting readback

APPLICATIONS

Mechanical potentiometer replacement
Instrumentation: gain, offset adjustment
Programmable voltage to current conversion
Programmable filters, delays, time constants
Programmable power supply
Low resolution DAC replacement
Sensor calibration

GENERAL DESCRIPTION

The AD5293 is a single-channel, 1,024-position digital potentiometer[1] with less than 1% end-to-end Resistor Tolerance error. The AD5293 performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. This device is capable of operating at high-voltages; supporting both dual supply ±10.5 to ±15V and single supply operation +21V to +30V.

The AD5293 offers guaranteed industry leading low resistor tolerance errors of ±1% with a nominal temperature coefficient of 35 ppm/°C. The low resistor tolerance feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

FUNCTIONAL BLOCK DIAGRAM

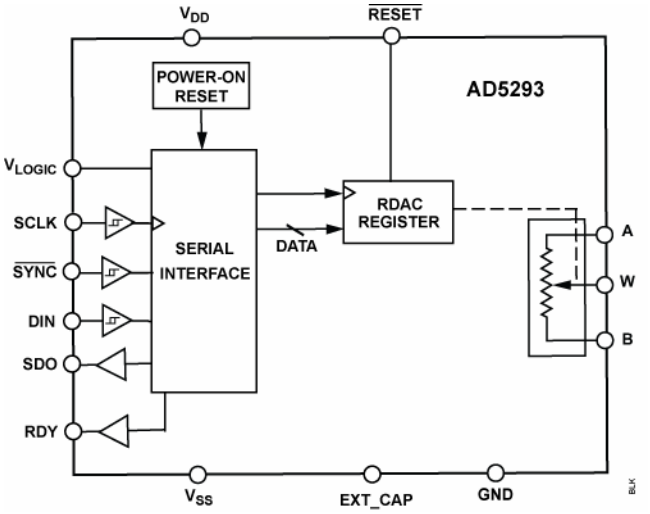

Figure 1. 14ld TSSOP

The AD5293 is available in a compact 14ld TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +105°C.

[1] The terms digital potentiometer and RDAC are used interchangeably.

Rev. PrA

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REVISION HISTORY

Revision: Preliminary Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS – 20KΩ VERSION

V_{DD} = 21V to 30V, V_{SS} = 0V; V_{DD} = 10.5V to 16.5V, V_{SS} = -10.5V to -16.5V; V_{LOGIC} = 2.7V to 5.5V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS— RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} = 20KΩ, $\|V_{DD} - V_{SS}\|$ = 26V to 30V	−1.5		+1.5	LSB
	R-INL	R_{AB} = 20KΩ, $\|V_{DD} - V_{SS}\|$ = 21V to 26V	−2		+2	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$		−1	0.5	+1	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W			TBD	TBD	Ω
DC CHARACTERISTICS— POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[4]	DNL		−1		+1	LSB
Integral Nonlinearity[4]	INL		−1		+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half-scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		TBD	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, Code = half-scale		50		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = half-scale		40		pF
Common-Mode Leakage Current[6]	I_{CM}	$V_A = V_B = V_W$		0.001	50	nA
DIGITAL INPUTS			JEDEC compliant			
Input Logic High	V_{IH}	V_{LOGIC} = 4.5V to 5.5 V	2.0			V
	V_{IH}	V_{LOGIC} = 2.7V to 3.6 V	1.8			V
Input Logic Low	V_{IL}	V_{LOGIC} = 2.7V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
DIGITAL OUTPUTS(SDO and RDY)						
Output High Voltage	V_{OH}	R_{PULL_UP} = 2.2kΩ to V_{LOGIC}	V_{LOGIC} - 0.4			V
Output Low Voltage	V_{OL}	R_{PULL_UP} = 2.2kΩ to V_{LOGIC}			Gnd +0.4V	V
Three state Leakage Current			-1		1	µA
Output Capacitance[6]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	21		30	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±10.5		±16.5	V
Positive Supply Current	I_{DD}	V_{DD} / V_{SS} = ±16.5 V		TBD	TBD	µA
Negative Supply Current	I_{SS}	V_{DD} /V_{SS} = ±16.5 V		TBD	TBD	µA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V; V_{IH} = 5 V or V_{IL} = GND		TBD	TBD	µA
	I_{LOGIC}	V_{LOGIC} = 3 V; V_{IH} = 3 V or V_{IL} = GND		TBD	TBD	µA
Memory Read Current[6,7]	$I_{LOGIC\_FUSE\_READ}$	V_{IH} = 5 V or V_{IL} = GND		TBD		mA

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		TBD	TBD	µW
Power Supply Rejection Ratio[6]	PSSR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%		0.0006	0.002	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth	BW	−3 dB		TBD		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 20 kΩ		-90		dB
		R_{AB} = 50 kΩ		-99		
		R_{AB} = 100 kΩ		-99		
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band,				
		R_{AB} = 20 kΩ		1		µs
		R_{AB} = 50 kΩ		2.5		
		R_{AB} = 100 kΩ		5		
Resistor Noise Density	e_{N_WB}	R_{WB} = 5 kΩ, T_A = 25°C,		TBD		nV/$\sqrt{Hz}$

[1] Typicals represent average readings at 25°C,V_{DD} = 15 V, V_{SS} = -15 V and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] ±1% resistor tolerance code range; R_{AB} = 20KΩ: 250 to 1,023 for $|V_{DD} - V_{SS}|$ = 26V to 30V and 383 to 1,023 for $|V_{DD} - V_{SS}|$ = 21V to 26V
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[6] Guaranteed by design and not subject to production test.
[7] Different from operating current; supply current for fuse read lasts approximately TBDµs..
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS}) + (I_{LOGIC} \times V_{LOGIC})$.
[9] All dynamic characteristics use V_{DD} = +15 V, V_{SS} = −15 V and V_{LOGIC} = 5 V.

ELECTRICAL CHARACTERISTICS – 50KΩ AND 100KΩ VERSIONS

V_{DD} = 21V to 30V, V_{SS} = 0V; V_{DD} = 10.5V to 16.5V, V_{SS} = -10.5V to -16.5V; V_{LOGIC} = 2.7V to 5.5V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS— RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL		−1		+1	LSB
Nominal Resistor Tolerance[3]	$\Delta R_{AB}/R_{AB}$		−1	0.5	+1	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$			35		ppm/°C
Wiper Resistance	R_W			TBD	TBD	Ω
DC CHARACTERISTICS— POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[4]	DNL		−1		+1	LSB
Integral Nonlinearity[4]	INL		−1		+1	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half-scale		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−6		0	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		TBD	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] A, B	$C_{A, B}$	f = 1 MHz, measured to GND, Code = half-scale		50		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = half-scale		40		pF
Common-Mode Leakage Current[6]	I_{CM}	$V_A = V_B = V_W$		0.001	50	nA
DIGITAL INPUTS			JEDEC compliant			
Input Logic High	V_{IH}	V_{LOGIC} = 4.5V to 5.5 V	2.0			V
	V_{IH}	V_{LOGIC} = 2.7V to 3.6 V	1.8			V
Input Logic Low	V_{IL}	V_{LOGIC} = 2.7V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
DIGITAL OUTPUTS(SDO and RDY)						
Output High Voltage	V_{OH}	R_{PULL_UP} = 2.2kΩ to V_{LOGIC}	V_{LOGIC} - 0.4			V
Output Low Voltage	V_{OL}	R_{PULL_UP} = 2.2kΩ to V_{LOGIC}			Gnd +0.4V	V
Three state Leakage Current			-1		1	µA
Output Capacitance[6]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	21		30	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±10.5		±16.5	V
Positive Supply Current	I_{DD}	V_{DD} / V_{SS} = ±16.5 V		TBD	TBD	µA
Negative Supply Current	I_{SS}	V_{DD} /V_{SS} = ±16.5 V		TBD	TBD	µA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V; V_{IH} = 5 V or V_{IL} = GND		TBD	TBD	µA
	I_{LOGIC}	V_{LOGIC} = 3 V; V_{IH} = 3 V or V_{IL} = GND		TBD	TBD	µA
OTP Read Current[6,7]	$I_{LOGIC\_FUSE\_READ}$	V_{IH} = 5 V or V_{IL} = GND		TBD		mA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		TBD	TBD	µW
Power Supply Rejection Ratio[6]	PSSR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%		0.0006	0.002	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth	BW	−3 dB		TBD		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz				
		R_{AB} = 20 kΩ		-90		dB
		R_{AB} = 50 kΩ		-99		
		R_{AB} = 100 kΩ		-99		
V_W Settling Time	t_S	V_A = 10 V, V_B = 0 V, ±1 LSB error band,				
		R_{AB} = 20 kΩ		1		µs
		R_{AB} = 50 kΩ		2.5		
		R_{AB} = 100 kΩ		5		
Resistor Noise Density	e_{N_WB}	R_{WB} = 5 kΩ, T_A = 25°C,		TBD		$nV/\sqrt{Hz}$

[1] Typicals represent average readings at 25°C,V_{DD} = 15 V, V_{SS} = -15 V and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] ±1% resistor tolerance code range; R_{AB} = 50KΩ: 128 to 1,023 for $|V_{DD} - V_{SS}|$ = 26V to 30V and 172 to 1,023 for $|V_{DD} - V_{SS}|$ = 21V to 26V; R_{AB} = 100KΩ: 83 to 1,023 for $|V_{DD} - V_{SS}|$ = 26V to 30V and 105 to 1,023 for $|V_{DD} - V_{SS}|$ = 21V to 26V;
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminals A, B, and W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[6] Guaranteed by design and not subject to production test.
[7] Different from operating current; supply current for fuse read lasts approximately TBDµs..
[8] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS}) + (I_{LOGIC} \times V_{LOGIC})$.
[9] All dynamic characteristics use V_{DD} = +15 V, V_{SS} = −15 V and V_{LOGIC} = 5 V.

INTERFACE TIMING SPECIFICATIONS

V_{DD} / V_{SS} = ±15 V, V_{LOGIC} = 2.7V to 5.5V, and −40°C < T_A < + 105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Unit[1]	Unit	Test Conditions/Comments
t_1[2]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	15	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	TBD	µs min	Minimum $\overline{SYNC}$ high time
t_9	13	ns min	$\overline{SYNC}$ rising edge to next SCLK fall ignore
t_{10}[3]	TBD	ns min	RDY rise to $\overline{SYNC}$ falling edge
t_{11}[3]	TBD	ns min	$\overline{SYNC}$ rise to RDY fall time
t_{12}[3]	TBD	ns min	RDY Low Time – RDAC Register write command execute time
t_{13}[3]	TBD	ns min	RDY Low Time – RDAC Register read command execute time
t_{14}[3]	125	ns max	SCLK rising edge to SDO valid
t_{15}[3]	TBD(40)	ns min	SCLK to SDO Data hold time
t_{OTP}	TBD	µs max	Power-on OTP restore time

[1] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency is 50 MHz
[3] R_{PULL_UP} = 2.2kΩ to V_{LOGIC}

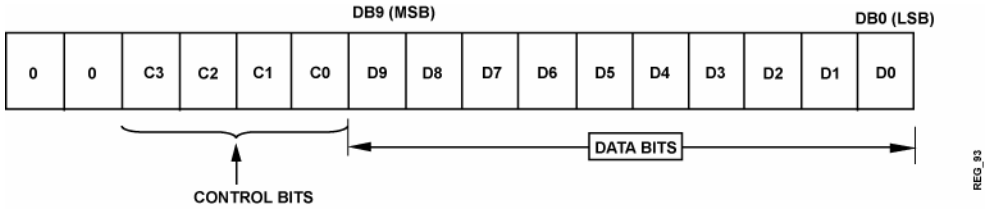

Figure 2. AD5293 Input Register Content

TIMING DIAGRAMS

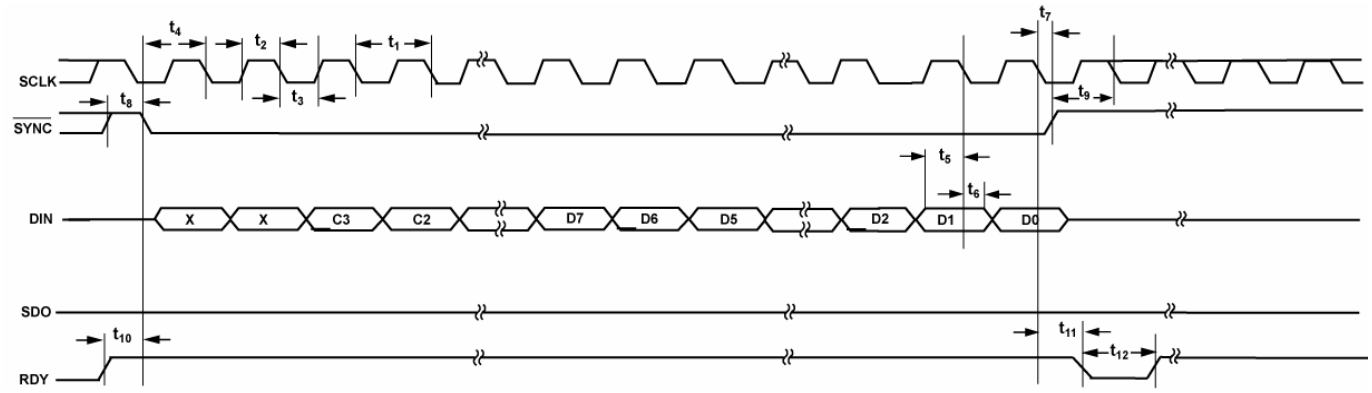

Figure 3. Write Timing Diagram

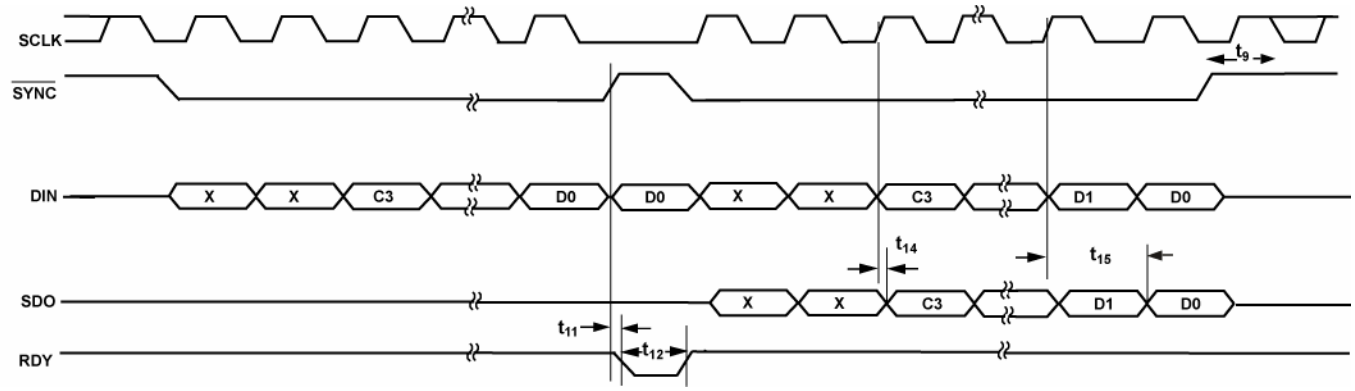

Figure 4. Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V, +35 V
V_{SS} to GND	+0.3 V, –16.5 V
V_{LOGIC} to GND	-0.3 V to +7 V
V_{DD} to V_{SS}	35 V
V_A, V_B, V_W to GND	V_{SS}–0.3 V, V_{DD}+0.3 V
I_A, I_B, I_W	
Pulsed[1]	±TBD mA
Continuous	
20KΩ End-to-End resistance	±3 mA
50KΩ and 100 KΩ End-to-End resistance	±2 mA
Digital Input and Output Voltage to GND	-0.3 V to V_{LOGIC} +0.3 V
Operating Temperature Range	–40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	–65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at peak temperature	20 sec to 40 sec
Thermal Resistance Junction-to-Ambient[2] θ_{JA},TSSOP-14	93°C/W
Thermal Resistance Junction-to-Case[3] θ_{JC}, TSSOP-14	20°C/W
Package Power Dissipation	(T_J max – T_A)/θ_{JA}

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Thermal Resistance (JEDEC 4 layer(2S2P) board).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

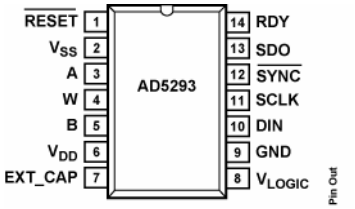

Figure 5. 14-pin TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Hardware reset pin. Sets the RDAC register to midscale. $\overline{\text{RESET}}$ is activated at the logic high transition. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if not used.
2	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$
4	W	Wiper terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$
5	B	Terminal B of RDAC. $V_{SS} \le V_B \le V_{DD}$
6	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
7	EXT_CAP	Connect a 1µF capacitor to EXT_CAP.
8	V_{LOGIC}	Logic Power Supply; 2.7V to 5.5V. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
9	GND	Ground Pin, Logic Ground Reference.
10	DIN	Serial Data Input. This part has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	$\overline{\text{SYNC}}$	Falling edge Synchronisation signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The selected DAC register is updated on the rising edge of $\overline{\text{SYNC}}$ following the 16th clock cycle. If $\overline{\text{SYNC}}$ is taken high before the 16th clock cycle the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. Open Drain Output requires external pull-up resistor. SDO can be used to clock data from the serial register in daisy chain or readback mode.
14	RDY	Ready pin. Active-high open-drain output. Identifies the completion of a write or read operation to/from the RDAC Register or read operation from memory Memory.

THEORY OF OPERATION

The AD5293 digital potentiometer is designed to operate as a true variable resistor for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The RDAC register can be programmed with any position setting using the standard SPI serial interface by loading the 16-bit data-word.

The AD5293 also features a patented 1% end-to-end resistor tolerance. This simplifies precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

RDAC REGISTER

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal B of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed. The RDY pin can be used to monitor the completion of a write to or read from the RDAC register. Prior to 20-TP activation, the AD5293 presets to mid-scale on power-up.

WRITE PROTECTION

On power-up, the serial data input register write command for the RDAC register is disabled. The RDAC write protect bit, C1 of the control register (Table 8), is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed to midscale using the software reset command (command #3) or through hardware by the $\overline{\text{RESET}}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register) the write protect bit C1 of the control register must first be programmed. This is accomplished by loading the serial data input register with Command #4 (Table 7).

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the serial data input register with Command #1 (Table 7) and the desired wiper position data. The $\overline{\text{RDY}}$ pin can be used to monitor the completion of this RDAC register write command. (Command #2, Table 7) can be used to readback the contents of the RDAC register. After issuing the readback command the $\overline{\text{RDY}}$ pin can be monitored to indicate when the data is available to be read out on SDO in the next SPI operation. Instead of monitoring the $\overline{\text{RDY}}$ pin, a minimum delay(Table 3) can be implemented when executing a write or read command. Table 6, provides an example listing of a sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format for an RDAC write and read.

Table 6. RDAC Register Write and Read

DIN	SDO	Action
0x1802	0xXXXX	Enable update of wiper position
0x0600	0x1803	Write 0x100 to the RDAC register, Wiper moves to ¼ fullscale position.
0x0800	0x0600	Prepare data read from RDAC Register
0x0000	0x0100	NOP instruction 0 sends 16-bit word out of SDO, where last 10-bits contain the contents of the RDACl Register.

POWER-DOWN MODE

The AD5293 can be powered down by executing the software powerdown command, command 6 (Table 7), and setting the LSB to 1. This feature reduces the power supply current to (TBD) μA and places the RDAC in a zero-power-consumption state where Terminal Ax is open-circuited and the Wiper Wx is connected to Terminal Bx.

RESET

A low to high transition of the hardware $\overline{\text{RESET}}$ pin loads the RDAC Register with midscale. The AD5293 can also be reset through software by executing command 3(Table 7).

SERIAL DATA INTERFACE

The AD5293 contains a serial interface ($\overline{\text{SYNC}}$, SCLK, DIN and SDO), which is compatible with SPI interface standards, as well as most DSPs. This device allows writing of data via the serial interface to every register.

INPUT SHIFT REGISTER

For the AD5293 the input shift register is 16 bits wide (see Figure 2). The 16-bit word consists of two unused bits (should be set to zero), followed by four control bits, and ten RDAC data bits. Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command (Table 7). Figure 3 shows a timing diagram of a typical AD5293 write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word is loaded from the DIN pin. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the instructions in Table 7. The command bits (Cx) control the operation of the digital

potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The AD5293 has an internal counter that counts a multiple of 16 bits (a frame) for proper operation. For example, the AD5293 works with a 32-bit word, but it cannot work properly with a 31-bit or 33-bit word. The AD5293 does not require a continuous SCLK and dynamic power can be saved by only transmitting clock pulses during a serial write. All interface pins should be operated at close to the supply rails to minimize power consumption in the digital input buffers.

DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes. It can be used to read the contents of the wiper setting using Command 2 (Table 7) or it can be used for daisy chaining multiple devices. The remaining instructions are valid for daisy-chaining multiple devices in simultaneous operations. Daisy-chaining minimizes the number of port pins required from the controlling IC. The SDO pin contains an open-drain N-Ch FET that requires a pull-up resistor, if this function is used. As shown in Figure 6, users need to tie the SDO pin of one package to the DIN pin of the next package. Users might need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO–DIN interface might require additional time delay between subsequent devices.

When two AD5293s are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1. The $\overline{\text{SYNC}}$ pin should be kept low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

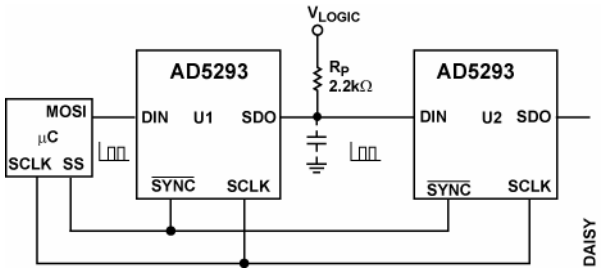

Figure 6. Daisy-Chain Configuration Using SD

Table 7. Command Operation Truth Table

Command Number	Command				Data										Operation
	B13				B9			B8	B7					B0	
	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP: Do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read RDAC wiper setting from SDO output in the next frame.
3	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Reset: Refresh RDAC with midscale code
4	0	1	1	0	X	X	X	X	X	X	X	D2	D1	D0	Write Contents of Serial Register Data to Control Register
5	0	1	1	1	X	X	X	X	X	X	X	X	X	X	Read Control Register from SDO output in the next frame.
6	1	0	0	0	X	X	X	X	X	X	X	X	X	D0	Software Powerdown D0 = 0; Normal Mode D0 = 1; Device placed in powerdown mode

Table 8. Control Register and special function codes

Register Name	Data Byte D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	Operation
Control	X X X X X X X C2 C1 X	C1 = RDAC Register Write Protect. 0 = Wiper position frozen to Midscale(Default) 1 = Allow update of wiper position through Digital Interface C2 = Calibration Enable. 0 = RDAC Resistor Tolerance Calibration enabled(Default) 1 = RDAC Resistor Tolerance Calibration enabled

RDAC ARCHITECTURE

In order to achieve optimum cost performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5293 employs a 3-stage segmentation approach as shown in Figure 7. The AD5293 wiper switch is designed with the transmission gate CMOS topology and with the gate voltage derived from V_{DD}.

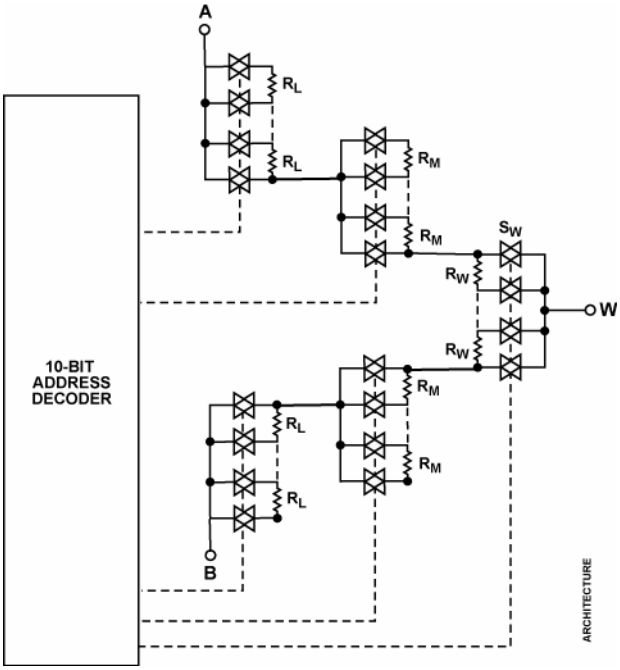

Figure 7. AD5293 Simplified RDAC Circuit.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation - 1% Resistor Tolerance

The AD5293 operates in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be floating or tied to the W terminal as shown in Figure 8.

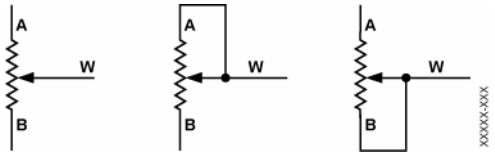

Figure 8. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is available in 20 kΩ, 50 kΩ, and 100 kΩ and has 1,024 tap points accessed by the wiper terminal. The 10-bit data in the RDAC latch is decoded to select one of the 1,024 possible wiper settings. The AD5293 contains an internal ±1% resistor tolerance calibration feature which can be disabled or enabled, enabled by default, by programming bit C2 of the control register (Table 8). The digitally programmed output resistance between the W terminal and the A terminal, R_{WA} and the W terminal and B terminal, R_{WB}, is calibrated to give a maximum of ±1% absolute resistance error over both the full supply and temperature ranges. As a result, the general equation for determining the digitally programmed output resistance between the W terminal and B terminal is

$$R_{WB}(D) = \frac{D}{1{,}024} \times R_{AB} \qquad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.
R_{AB} is the end-to-end resistance.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} is also calibrated to give a maximum of 1% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equation for this operation is

$$R_{WA}(D) = \frac{1{,}024 - D}{1{,}024} \times R_{AB} \qquad (2)$$

where:
D is the decimal equivalent of the binary code loaded in the 10-bit RDAC register.
R_{AB} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of TBD Ω is present. Regardless of which setting the part is operating in, care should be taken to limit the current between the A terminal to B terminal, W terminal to A terminal, and W terminal to B terminal, to the maximum continuous current of ±3 mA(20KΩ) or ±2 mA(50KΩ and 100 KΩ) or pulse current of TBD mA. Otherwise, degradation, or possible destruction of the internal switch contact, can occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper to B and wiper to A proportional to the input voltage at A to B as shown in Figure 9. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

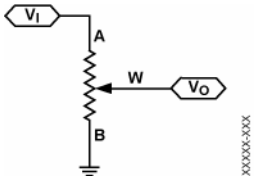

Figure 9. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for simplicity, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B

ranging from 0 V to 1 LSB less than 30 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B, divided by the 1,024 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{1{,}024} \times V_A + \frac{1{,}024 - D}{1{,}024} \times V_B \qquad (3)$$

In voltage divider mode, to optimize wiper position update rate, it is recommended to disable the internal ±1% resistor tolerance calibration feature by programming bit C2 of the control register (able 9).

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

EXT_CAP CAPACITOR

A 1µF capacitor to GND must be connected to the EXT_CAP pin (Figure 10) on power-up and throughout the operation of the AD5293.

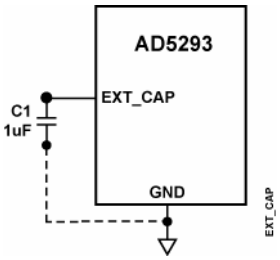

Figure 10. Hardware setup for EXT_CAP pin

TERMINAL VOLTAGE OPERATING RANGE

The AD5293's positive V_{DD} and negative V_{SS} power supplies define the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminals A, B, and W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 11).

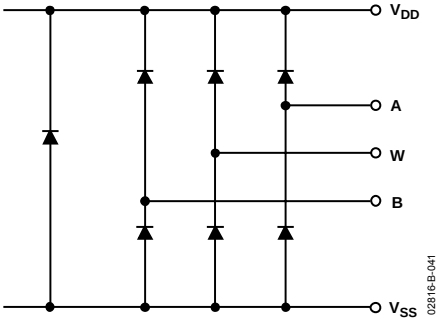

Figure 11. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5293 device is primarily used as a digital ground reference. To minimize the digital ground bounce, the AD5293 ground terminal should be joined remotely to the common ground. The digital input control signals to the AD5293 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the Specifications section.

Power-Up Sequence

Because there are diodes to limit the voltage compliance at Terminals A, B, and W (Figure 11), it is important to power V_{DD}/V_{SS} first before applying any voltage to Terminals A, B, and W. Otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. The ideal power-up sequence is GND, V_{DD}/V_{SS}, V_{LOGIC}, digital inputs, and V_A, V_B, and V_W. The order of powering V_A, V_B, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS} and V_{LOGIC}.

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{LOGIC} is powered, the power-on preset activates, which restores midscale to the RDAC register.

OUTLINE DIMENSIONS

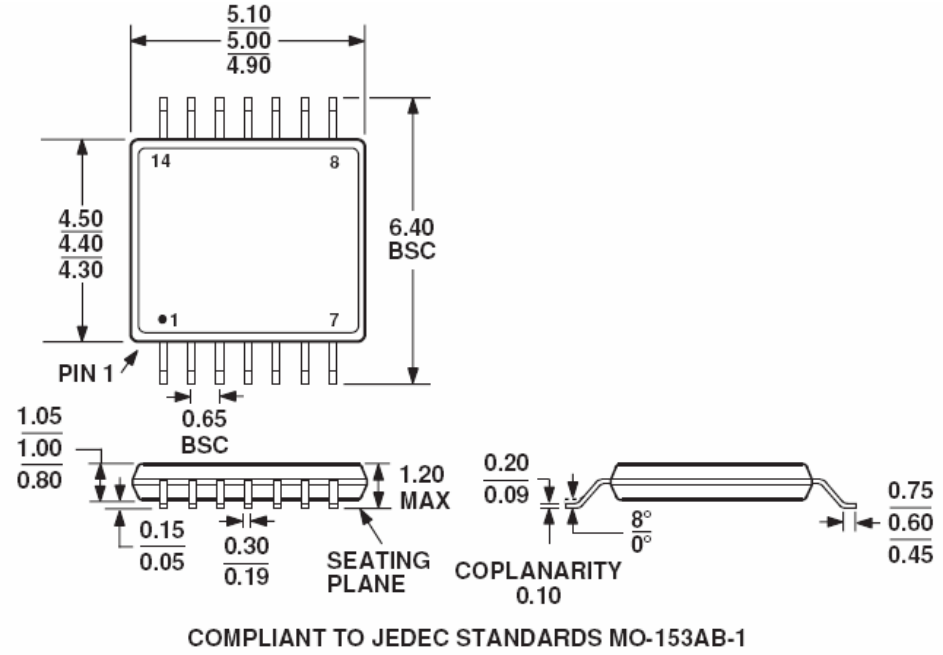

Figure 12. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option
AD5293ABRUZ20	20	1,024	–40°C to +105°C	14-Lead TSSOP	RU-14
AD5293ABRUZ50	50	1,024	–40°C to +105°C	14-Lead TSSOP	RU-14
AD5293ABRUZ100	100	1,024	–40°C to +105°C	14-Lead TSSOP	RU-14

PR07675-0-7/08(PrA)